

Alternative UBM for Lead Free Solder Bumping using C4NP

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Abstract

Microelectronic packaging continues the migration from wire bond to flip chip first level interconnect (FLI) to meet aggressive requirements for improved electrical performance, reduced size and weight. The interconnect pitch is being predicted by forecasts like ITRS to be reduced to 100 um and below for full array I/O layout. For wafer bumping, solder electroplating is commonly employed, especially for fine pitch applications. Wafer level chip scale packaging (WLCSP) typically utilizes solder sphere placement technology to manufacture the bumps. In WLCSP, pitch and solder ball size are usually much higher and the number of I/O much lower than for Flip Chip in Package (FCiP) applications. C4NP (Controlled Collapse Chip Connection New Process) has proven to be suitable for a broad range of solder bump pitches, encompassing FCiP to CSP bump dimensions. As the industry migrates to 300mm wafer processing and lead-free flip chip interconnect, C4NP is establishing itself as a viable solder bumping alternative. Due to its nature as a bump transfer technology, it is expected that the bumping yield will be very high, since filled molds can be inspected prior to solder transfer to the wafer. Yield is a major issue for the highest I/O applications like microprocessors.

The under bump metallurgy (UBM) structure is a critical component of any solder interconnect system. The UBM typically provides three functions: adhesion to underlying dielectric and metal, barrier to protect the silicon circuitry, and a solder wettable surface. For lead-free bumps, the barrier layer is key to the reliability of the solder joint due to the higher Sn content in the lead free solder. A common barrier layer used in the industry is electroplated nickel. This layer provides good protection from degradation of the silicon metallurgy by tin rich lead free solders. C4NP provides an opportunity to eliminate electroplating, and its associated costs for plating chemistry, analysis, supply and waste treatment.

This paper analyzes two alternative UBM structures: sputtered TiW/Ni and electroless Ni/immersion Au (ENIG), with and without Pd. Wafers were fabricated with these UBM structures, solder applied with C4NP, and chip level stressing performed to determine the robustness of these alternative stack-ups. Analysis of these structures following multiple reflows and thermal cycling is presented.

In addition, the work also discusses production cost analysis based on a cost model specifically developed to determine manufacturability of the various UBM structures.

C4NP is a novel solder bumping technology developed by IBM which addresses the limitations of existing bumping

technologies by enabling low-cost, fine pitch bumping using a variety of lead-free solder alloys. It is a solder transfer technology where molten solder is injected into pre-fabricated and reusable glass molds. The glass mold contains etched cavities which mirror the bump pattern on the wafer. The filled mold is inspected prior to solder transfer to the wafer to ensure high final yields. Filled mold and wafer are brought into close proximity/soft contact at reflow temperature and solder bumps are transferred onto the entire 300mm (or smaller) wafer in a single process step without the complexities associated with liquid flux.

The data in this paper is provided by the analytical laboratory at Fraunhofer Institute, IZM, Berlin, Germany. UBM formation was done at NEXX Systems, Billerica, MA and Fraunhofer IZM. Wafer bumping was done using the C4NP process at the IBM Hudson Valley Research Park.

UBM Technology Overview

The Under Bump Metallization (UBM) is the direct interface between the interconnecting solder and the final chip metallization [1]. The UBM has to provide a low resistance contact between the chip pad and the solder, good adhesion to the chip metallization and the chip passivation and a hermetic seal between the UBM and IC pad. It has to be a reliable diffusion barrier between the IC pad and bump with low film stress and it needs to be sufficiently resistant to stress caused by thermal mismatch during die assembly. In the case of PbSn bumping, common UBM stacks are Cr-Cr:Cu-Cu-Au (original C4 from IBM); Ti-Cu; Ti:W-Cu; Ti-Ni:V; Cr-Cr:Cu-Cu; Al-Ni:V-Cu; Ti:W(N)-Au. Usually, these UBM stacks are sequentially deposited by sputtering or plating.

Intermetallic compounds (IMCs) are formed between Sn and Cu or Ni by the reflow process providing the required adhesion of the bump to the chip pad. IMCs are brittle in nature due to the ordered crystal structure which is in contrast to the solid solutions. The metals which are mostly used in packaging; Cu, Ni, Au and Pd; form binary intermetallics with Sn-based solders of the Hume Rothery type.

In general, the intermetallic growth rate with Sn is much higher for Cu compared to Ni. This is becoming more important for lead-free solders due to their higher Sn content.

As previously described, the barrier integrity provided by the UBM structure is of critical importance for the performance of lead free solders. A common barrier layer used for electroplated lead free solder is electroplated Ni. C4NP provides the opportunity to eliminate electroplating of solder. If electroplating of the UBM can be avoided, the entire infrastructure required for electroplating chemistry

procurement, analysis, mixing, pumping and waste treatment can be avoided. A detailed cost model has been developed, which shows that these electroplating infrastructure costs are a significant portion of the overall bumping cost for a wafer.

Two approaches, described in this paper, for avoiding electroplating of the UBM structure are:

1. An electroless Ni/immersion Au (ENIG) UBM, with or without electroless Pd

2. A sputtered TiW/Ni UBM

ENIG is a well known and commonly practiced UBM for lead free solders. It has the advantage of not requiring photolithography to form a “capture pad” for the C4NP solder transfer process. The ENIG metallurgy is simply applied directly on the wafer metallurgy in the passivation layer via, and then solder is applied with C4NP. The alternative, all sputtered, UBM (TiW/Ni) has the advantage of not requiring any plating chemistry, analysis or waste treatment. However, photolithography is still required to form a capture pad for C4NP solder transfer.

A description of the ENIG vs sputtered UBM process is described in Figure 1.

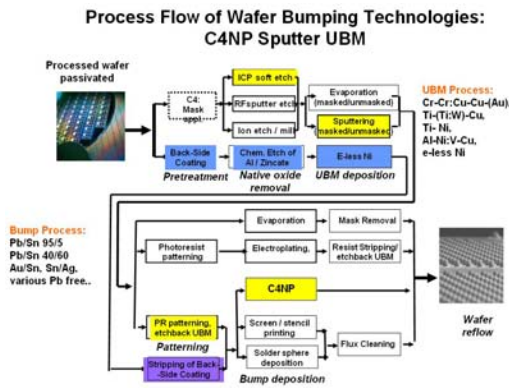


Figure 1: ENIG vs sputtered UBM process description

Electroless Nickel UBM

The ENIG process is based on the selective chemical deposition of metal on Al bondpads. Wafers are treated in a sequence of chemical solutions. After each treatment they have to be rinsed carefully in DI water. The principle of the process is shown in Figure 2. First the surface of Al bondpads are cleaned by immersing the wafers into two baths. The first (passivation cleaner) removes possible residues while the second (Al cleaner) removes thick Al oxides and roughens the surface. In a zincate bath a thin Zn layer is deposited on Al by an exchange reaction in order to activate the surface for subsequent Ni plating. The electroless Ni bath contains mainly Ni ions and hypophosphite. A first Ni layer is deposited on the pads by an exchange reaction between Zn and the Ni ions. On this first layer additional Ni is plated by a continuous autocatalytic reaction. The plating rate is 25 $\mu\text{m/hr}$. In the subsequent immersion Au solution, a thin Au film is deposited by an exchange reaction on the surface of the Ni layer. The Au has a thickness of 0.05 – 0.08 μm and is required to prevent Ni from oxidation.

The complete process flow is shown in Table 1. In addition to the wet chemical treatments mentioned above, the backsides of the wafers have to be protected in order to

prevent Ni deposition on Si. This is done by spin-coating of a protective resist on the backside of the wafer. After bump plating, the resist is stripped. All chemicals used in this process are commercially available. They are completely cyanide-free and no organic solvents are used.



Figure 2: Principle process of electroless Ni bumping: (a) bondpad in initial state, (b) after zinc deposition, (c) after growth of electroless Ni, (d) after plating of thin immersion Au.

process step	function
1. protective resist coating	protective resist coating on wafer backside
2. passivation cleaning	removes passivation residues from Al pads
3. Al cleaning	removes thick Al oxides and prepares surface for metal deposition
4. zincating	activates Al for Ni deposition
5. electroless Ni	deposition of Ni layer (typ. 5 μm)
6. immersion Au	Au finish on Ni (typ. 0.08 μm) to prevent Ni from oxidation
7. backside cleaning	removes protective coating from backside

Table 1: Process steps of electroless Ni bumping and their function.

For all wet-chemical treatments, 25 wafers are handled together in one carrier. The process requires tanks with seven different chemical baths and additional rinse tanks. The process times are relatively short. They have a range from 30 s (zincating) to 30 min (immersion Au). By handling the wafer cassettes manually from bath to bath a throughput of 25 wafers per hour can be achieved. In fully automatic systems 100 wafer per hour are possible.

The uniformity of the Ni height is better than $\pm 5\%$ over a 200 mm wafer. The variation within a die is correspondingly lower.

Sputtered Ni UBM

The sputtered UBM films were deposited using the NEXX Systems Nimbus XP. TiW was deposited at a sputtering pressure of 7 mTorr to reduce compressive stress [2]. Nickel was deposited at a sputtering pressure of 2 mTorr using a Ni magnetron designed specifically for sputtering of magnetic Ni. RF Bias was used on half of the samples to reduce tensile stress in Ni films. The microstructure of Ni films deposited with and without substrate bias is significantly different [3]. In the case of Ni films deposited without substrate bias, the grain size is of the order of the film thickness (0.5 to 1.5 microns). In Ni films deposited with substrate bias, the grain size is considerably smaller, of the order of 50 – 100 nm. This

difference in microstructure is expected to influence the formation of intermetallic compounds during initial reflow of C4 bumps and subsequent reliability testing.

Wafers were patterned using Clariant Novolack AZ 4562 Photoresist. Resist thickness was 30 um with a standard deviation of less than 1% over 200 mm with an edge exclusion of 3.5 mm. Mask aligner technology (MA 200, SüssMicrotec) was used for the lithography. The AZ 4562 was developed using aqueous AZ 400K. Resist stripping was done in a single wafer Raider SP from Semitool using organic solvents. The Ni was etched using a proprietary etching solution from Fraunhofer IZM.

C4NP Technology Overview

The C4NP process starts with a glass mold in which the bump pattern for an entire wafer is replicated as a mirror image of cavities in the glass mold. These cavities are filled with solder as the mold is scanned below a fill head. The fill head contains a reservoir of molten solder and a slot through which the solder is injected into the mold cavities. The cavity geometry determines the volume of the solder bumps that will be subsequently formed on the wafer. The filled mold is inspected automatically and then aligned below a wafer with exposed UBM pads facing the mold. Mold and wafer are heated above the solder melting point and then brought into contact. The solder forms spherical balls which transfer from the mold to the UBM regions on the wafer, where they preferentially wet and solidify. Wafer and mold are separated, and the mold is cleaned for reuse.

Description of Test Cells

Two UBM structures were evaluated. The first set consisted of varying thicknesses of electroless Ni, electroless Pd and immersion Au, as described in Table 2 below.

Ni	Pd	Au	Solder
3um	No	100nm	Sn/Cu
3um	No	100nm	Sn/Ag
7um	No	No	Sn/Cu
7um	No	No	Sn/Ag
7um	No	100nm	Sn/Cu
7um	No	100nm	Sn/Ag
7um	0.5um	100nm	Sn/Cu
7um	0.5um	100nm	Sn/Ag
15um	No	100nm	Sn/Cu
15um	No	100nm	Sn/Ag

Table 2: test matrix 1

The second set consisted of sputtered TiW and sputtered Ni, with and without the application of substrate bias during the deposition of the Ni layer, as described in Table 3.

TiW	Ni	Bias	Solder
200nm	0.5um	No	Sn/Cu
200nm	0.5um	No	Sn/Ag
200nm	0.5um	Yes	Sn/Cu
200nm	0.5um	Yes	Sn/Ag
200nm	1.0um	No	Sn/Cu
200nm	1.0um	No	Sn/Ag
200nm	1.0um	Yes	Sn/Cu
200nm	1.0um	Yes	Sn/Ag
200nm	1.5um	No	Sn/Cu
200nm	1.5um	No	Sn/Ag
200nm	1.5um	Yes	Sn/Cu
200nm	1.5um	Yes	Sn/Ag

Table 3: test matrix 2

For each test matrix, the Sn/Cu alloy used was Sn/0.7%Cu. The Sn/Ag was a proprietary alloy composition. The test chip is based on 3 um thick AlCu pads passivated with 7 um thick PI (HD 4000 series). The chip size is 15 mm x 15 mm square, 150 um pitch. The test chip is shown in Figure 3.

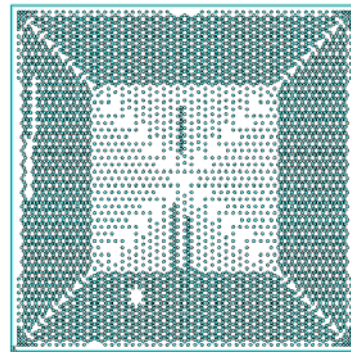


Figure 3: test chip

The AlCu pad size is 126 um and the opening in the polyimide is 54 um. In the case of the sputtered UBM, the UBM pad size is 126 um. In the case of the ENIG samples, the diameter of the Ni pad depends on the thickness of the electroless Ni.

Experimental Results

Table 4 provides ball shear results for test matrix 1. The C4 balls were sheared at a rate of 25um/sec at a height of 25um above the polyimide passivation surface. The average was calculated from 30 shear measurements from C4 bumps selected randomly across each chip. Data is provided for each cell at time zero and at one, three, five and ten lead free solder reflows. Samples at time zero have undergone only the C4NP process, with one solder reflow cycle (“as-received”).

Subsequently, the samples received 1, 3, 5, and 10 additional reflows in a nitrogen convection oven with a lead-free

temperature profile. Also provided is data for each cell after 100, 250, 500 and 1000 deep thermal cycles (-50 to + 125C).

Ni um	Pd um	Au nm	Solder	T0 (g)	1X (g)	3X (g)	5X (g)	10X (g)	100 cy (g)	250 cy (g)	500 cy (g)	1000 cy (g)
3	No	100	Sn/Cu	12.43	13.32	13.97	13.84	14.24	12.74	14.1	12.37	13.87
3	No	100	Sn/Ag	15.51	12.02	14.53	13.67	12.97	13.37	14.82	14.03	15.12
7	No	No	Sn/Cu	12.74	13.78	13.03	13.18	13.49	11.54	11.37	10.97	11.56
7	No	No	Sn/Ag	14.59	15.96	15.76	15.29	15.67	13.86	13.78	14.15	13.58
7	No	100	Sn/Cu	13.22	15.28	14.09	14.44	15	14.6	16.25	13.44	16.58
7	No	100	Sn/Ag	16.64	18.9	18.29	17.34	18.46	17.16	17.76	16.24	16.72
7	0.5	100	Sn/Cu	15.54	15.74	16.24	15.79	16.08	14.74	14.51	14.44	13.96
7	0.5	100	Sn/Ag	17.31	17.77	17.99	17.45	17.17	17.64	17.87	16.86	16.71
15	No	100	Sn/Cu	15.87	17.7	18.27	18.33	18.27	16.06	18.87	14.82	18.36
15	No	100	Sn/Ag	20.04	24.3	23.58	22.68	21.76	20.28	20.5	20.1	19.36

Table 4: Ball shear values for test matrix 1

Figure 4 shows a cross section of a C4 bump at time zero with 7um Ni and Sn/Ag solder.

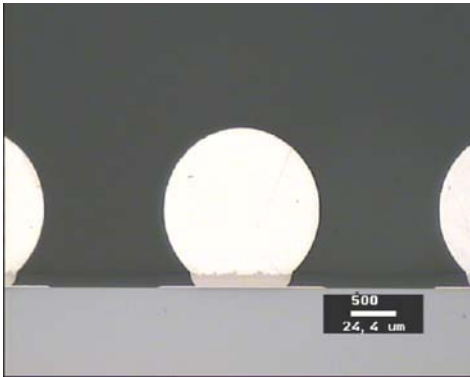


Figure 4: 7um Ni with Sn/Ag solder

Several observations can be made from this data:

1. The ball shear forces are roughly proportional to the UBM area. The greater the Ni thickness, the greater the resulting UBM pad diameter and resulting shear strength. It is expected that shear strength will increase with increasing pad area.
2. The shear force of Sn/Ag solder is in general greater than for Sn/Cu solder. This is expected, since Sn/Ag solder has a higher yield strength and hardness than Sn/Cu solder. Also, Ag₃Sn intermetallics strengthen the solder joint.
3. All ball shear failure modes were within the bulk solder. This may have changed if the shear height had been closer to the UBM pad.

4. Shear values are roughly stable through 10X reflows and 1000 thermal cycles. This UBM structure is very robust.

5. Au improves the ball shear strength, all else being equal.

6. Pd does not have a significant effect on the shear strength of the solder joints.

Table 5 provides ball shear values at time zero and after 100, 250 and 500 deep thermal cycles (-55 to +125C) for test matrix 2. The C4 balls were sheared at a rate of 25um/sec at a height of 25um above the polyimide passivation surface. The average was calculated from 15 shear measurements near the chip edge and 15 measurements at the chip center for each chip.

Several observations can be made from this data. First, the time zero shear strengths decrease as the Ni thickness increases. Second, the shear strength decreases more rapidly between time zero and 250 thermal cycles for the thinner Ni cells. Solder metallurgy and bias did not appear to have a significant effect on the results. Further work is underway to characterize these cells after additional thermal cycles.

Table 6 provides ball shear values at time zero and after an additional one, three, five and ten reflows for test matrix 2. The C4 balls were sheared at a rate of 25um/sec at a height of 25um above the polyimide passivation surface. The average was calculated from shear test values of six measurements.

TiW	Ni	Bias	Solder	Average of shear (g)			
				Time zero	After 100 cycles	After 250 cycles	After 500 cycles
nm	um						
200	0.5	No	SnCu	23.12	19.23	17.69	17.80
200	0.5	No	SnAg	27.27	21.52	22.30	23.51
200	0.5	Yes	SnCu	23.65	19.58	19.05	19.21
200	0.5	Yes	SnAg	26.73	23.77	22.50	22.29
200	1.0	No	SnCu	22.09	16.97	16.82	17.46
200	1.0	No	SnAg	21.57	21.27	21.01	21.18
200	1.0	Yes	SnCu	23.96	23.63	21.95	20.76
200	1.0	Yes	SnAg	19.21	18.27	17.13	17.08
200	1.5	No	SnCu	17.69	16.04	16.04	16.10
200	1.5	No	SnAg	16.75	N/A	N/A	N/A
200	1.5	Yes	SnCu	17.29	16.62	16.01	15.94
200	1.5	Yes	SnAg	18.63	14.14	18.89	N/A

Table 5: Ball shear values for test matrix 2 (thermal cycling)

TiW	Ni	Bias	Solder	Average of shear (g)				
				Time zero	1X	3X	5X	10X
nm	um							
200	0.5	No	SnCu	23.12	21.97	21.51	21.88	21.27
200	0.5	No	SnAg	27.27	25.75	25.35	24.01	24.02
200	0.5	Yes	SnCu	23.65	20.93	20.74	22.37	21.62
200	0.5	Yes	SnAg	26.73	27.75	24.00	24.00	24.36
200	1.0	No	SnCu	22.09	22.66	22.07	23.54	23.88
200	1.0	No	SnAg	21.57	23.45	24.79	23.74	24.02
200	1.0	Yes	SnCu	23.96	29.01	29.41	28.24	29.35
200	1.0	Yes	SnAg	19.21	23.19	21.11	23.45	23.58
200	1.5	No	SnCu	17.69	19.14	19.08	21.30	20.04

200	1.5	No	SnAg	16.75	N/A	N/A	N/A	N/A
200	1.5	Yes	SnCu	17.29	19.05	18.52	19.47	19.58
200	1.5	Yes	SnAg	18.63	17.84	N/A	N/A	N/A

Table 6: Ball shear values for test matrix 2 (multiple reflows)

The shear strengths tend to increase for the thicker Ni cells with increasing number of reflows. Further work is underway to characterize these cells.

Production Cost Analysis

There are two main aspects contributing to the per wafer cost of a lead-free solder bumping process: the cost to create the UBM stack and the cost of building the bump by depositing solder. Prior to C4NP, the most widely used manufacturing process for lead-free flip chip solder bumping was based on electroplating of both part of the UBM stack as well as the solder using a single lithographic layer for patterning. This sequence makes it difficult to draw a line between UBM and bump formation as shown in Figure 5.

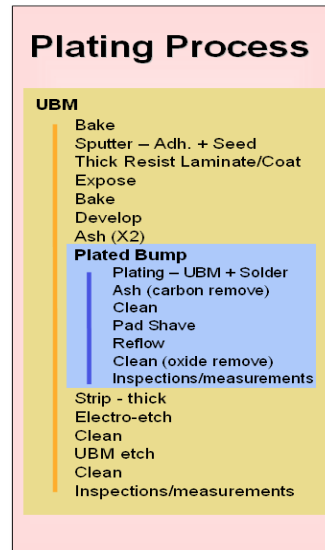


Figure 5 – Integrated UBM-BUMP process flow

The C4NP process is significantly different as it decouples UBM and bump formation entirely. The UBM stack is formed using any variety of UBM processes as described elsewhere in this paper. The bumps are formed using the C4NP process sequence. Figure 6 illustrates the UBM flexibility in combination with C4NP solder deposition.

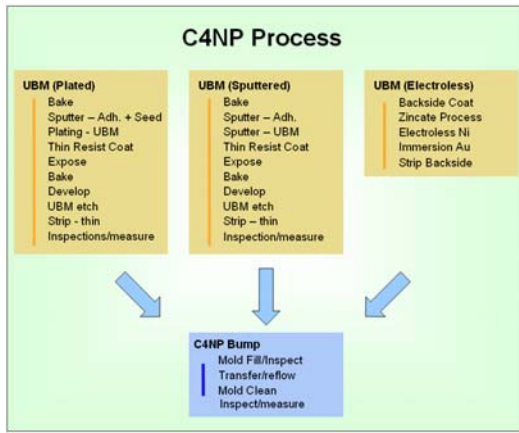


Figure 6 – UBM variety in conjunction with C4NP solder deposition method

This fundamental difference in process sequences manifests itself not only in per-wafer cost but also in non-cost related distinctions such as cycle time and process logistics.

The per wafer cost for production wafer bumping is a function of the following cost determining factors: personnel cost, consumable and material cost, equipment maintenance and support, equipment depreciation, building overhead as it relates to equipment footprint and cleanroom requirements, wafer yield, NRE cost per part number or bump pattern, chemistry supply, waste treatment and IP cost.

It would be beyond the scope of this paper to provide quantitative numbers for these various factors. However, Figure 7 summarizes a qualitative assessment of these parameters.

Cost Factor	Comment
Personnel cost	Operators, Engineers, Management, Administrative overhead
Consumable and material cost	Bulk solder, glass molds
Equipment maintenance and support	Equipment engineering, scheduled downtime
Equipment depreciation	Function of capital required
Building overhead	Function of footprint and clean-room quality required
Wafer yield	Function of process complexity, number of process steps
NRE cost per part number/bump pattern	Function of mask cost, mold cost, number of uses per mold, number of molds required
Chemistry supply	Function of solder composition and method of deposition
Waste treatment	Function of chemistry used
IP cost/IP wafer toll	Function of IP ownership

Figure 7 – Cost factors for wafer bumping line

As part of this work, a sophisticated cost model has been developed to investigate the impact of UBM cost on the overall per wafer bumping cost and to model the cost differences of the various UBM process methods described in this paper. Integrated Device Manufacturers (IDM) as well as bumping service providers have largely implemented some version of a plating process as described in figure 5. Assumptions were made as to the type of equipment used, its footprint and facility requirements as well as its capital cost and throughput. Data from several leading equipment suppliers and IDMs formed the basis for this model.

The results show that the UBM-BUMP cost ratio is approximately 2:1. In other words, over 60% of per wafer cost in a typical plated bumping line is driven by the cost of the UBM. This ratio obviously depends on the specifics of the process sequence as well as the type of equipment used. By

running the model under varying assumptions, the UBM-BUMP cost ratio ranged from 61%:39% to 75%:25%. From a process perspective, electroplating and photo lithography and their associated cost contributions had the biggest impact on overall per wafer bumping cost.

The results of modeling a typical wafer bumping line show that reducing the UBM cost will have the largest impact on overall per wafer cost.

Unlike a plated bumping line, C4NP bumping technology enables the use of alternative, lower cost UBM process sequences as outlined in figure 6. This paper focuses on the evaluation of a sputtered TiW/Ni UBM as well as an electroless Ni/immersion Au UBM which does not involve sputtering. No electroplating technology was utilized. Figure 8 illustrates the per wafer bumping cost results based on the various models. The cost numbers have been normalized in order to show the differences in the various processes without disclosing sensitive or proprietary information from tool and materials vendors. Furthermore, the absolute cost numbers also vary significantly based on regional parameters such as personnel and building cost. For the purpose of a cost comparison, a normalized view eliminates the effect of those parameters. The models were based on 300mm wafers with lead-free solder cost parameters.

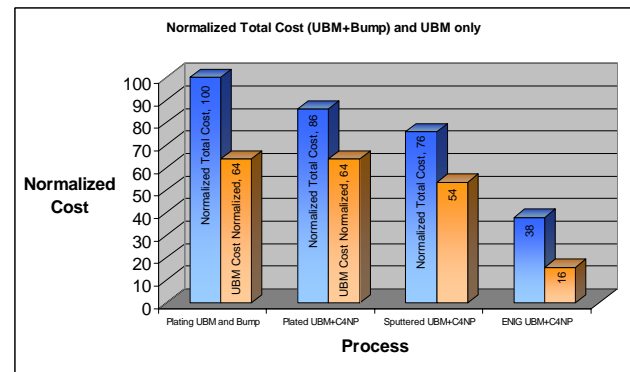


Figure 8: Total per-wafer cost and respective UBM portion of the cost

A traditional plated bumping line (“Plating UBM and Bump”) was modeled as the 100% reference. As outlined above, the UBM portion of the per-wafer cost is over 60%, 64% in this particular case. In comparison, the C4NP bumping line when used with a plated UBM (“Plated UBM+C4NP”) resulted in a 14% reduction in overall bumping cost. Although the overall cost reduction is significant, the relative cost of the UBM is even higher – 74% of the total per-wafer cost in this particular case. This is expected due to the necessary electroplating infrastructure in addition to C4NP. Eliminating electroplating all together by replacing the UBM process with an all sputtered metal stack (“Sputtered UBM+C4NP”) further reduced the per-wafer cost. UBM processing still accounts for about 71% of the total cost. However, the total cost is down to 76% compared to a traditional plated bumping line. Although lower than in the case of electroplating, UBM cost is still relatively high mainly due to the use of photo lithography. The model for electroless

Ni/immersion Au UBM (“ENIG UBM+C4NP) in combination with C4NP solder deposition showed the biggest impact on cost. The total per-wafer cost is reduced to 38% compared to the per-wafer cost of an electroplating bumping line. The UBM only accounts for 41% of that reduced cost.

In conclusion, the achievable cost reduction by utilizing a non-electroplated UBM in combination with C4NP is significant. The reduced cost is mainly driven by the elimination of electroplating and the reduced or eliminated use of photo lithography. Of course, each UBM construction must be evaluated to determine if it meets the reliability requirements for a given application.

One of the most fundamental differences between C4NP and alternative bumping technologies is the use of glass molds. A minimum number of molds are required depending on the number of wafers per day with a particular bump pattern. The cost of molds directly impacts the per wafer bumping cost. The number of reuses of a given mold is critical. Data in previous publications shows that C4NP molds can be used several hundred times before they have to be replaced. The various cost models above consider the impact of C4NP molds on the overall per-wafer cost.

Conclusions

Alternative UBM structures have been demonstrated with lead free solders applied with C4NP. The ENIG UBM structures tested have proven to be very robust, with minimal changes in shear strength after 10 reflows and 1000 deep thermal cycles. The thicker sputtered Ni structures have shown promising results as well. Significant cost savings are realized by using ENIG or sputtered Ni instead of electroplated Ni UBMs for lead free solders. This paper analyzed chip level data only. A rigorous reliability qualification must be performed, including first and second level interconnection, to determine if a given UBM and bump construction will meet the requirements for a given application.

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