

PVD Processing for Flip Chip

CONSIDERING ADHESION LAYER PROPERTIES

BY ARTHUR KEIGLER, STEPHEN GOLOVATO, PH.D., KATHY O'DONNELL, PH.D., JOHANNES CHIU, PH.D., AND RICHARD HOLLMAN, PH.D. NEXX Systems, Inc.

Advanced packaging processes use physical vapor deposition (PVD) for gold bumping, solder bumping, redistribution (RDL), and integrated passive components. A critical element of PVD is the initial layer that attaches the subsequent structures to the device elements. Titanium (Ti) and titanium-tungsten (TiW) are most commonly used for these applications. Table 1 gives an overview of typical PVD film stacks.

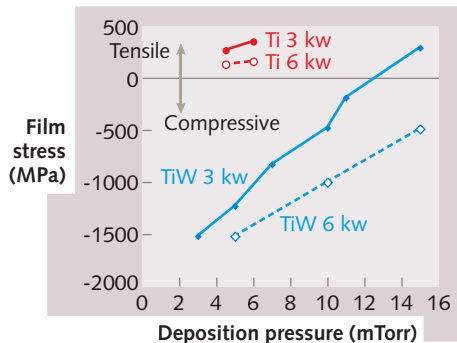


FIGURE 1. TiW and Ti film stress vs. deposition pressure for deposition powers of 3kw 6kw.

bonds, which provide a strong adhesion between the PVD film and the wafer.

The adhesion layer seals the internal pad/wiring of the device from the package-level wiring or bumping and the subsequent environment. Applications requiring higher reliability will use PVD to create this strong adhesion to the dielectric.

Several steps prior to PVD metal deposition improve the adhesion to the dielectric. A degas step, applied by exposing wafers to infrared illumination from a bank of heating lamps, drives out water from the dielectric material, which is especially necessary for hydrophilic organic dielectric materials.

THE SHORT STORY ■ PVD is the primary method for depositing under bump metallization (UBM) stacks. Material choice depends on several factors including adhesion, film stress, particle contamination, and cost-of-ownership. Process considerations must be made for optimizing Ti and TiW adhesion/barrier layers for UBM.

Functions of the Ti or TiW Layer

For plating seed layer applications, the PVD stack primarily provides the adhesion function to the underlying pad and dielectric, and a conductive layer for electroplating. For UBM applications, the PVD stack creates a barrier to gold or solder diffusion into the pad, and also creates an intermetallic bond to attach the subsequent bump. Because it requires a high vacuum system, PVD has been considered expensive. But process

tools designed specifically for packaging applications have helped fuel the industry's growth.

Adhesion Function

Adhesion to both metal pads and dielectric materials is the primary function of Ti or TiW layers. Ti is a well-known adhesion metal, due to its strong affinity for oxygen. For example, in a PVD chamber, a common practice for removing absorbed water after a preventive maintenance event is to sputter Ti into the chamber to scavenge absorbed water from the chamber walls. Electron transfer between titanium and oxygen in the top layers of the dielectric creates titanium-oxide

PVD film stack	Application	Typical thickness
TiW-Au	Gold bump UBM	TiW (3000A) – Au (1000A)
Ti-Cu TiW-Cu	Solder bump seed layer (Ni or thick Cu UBM plated on top) RDL seed layer Integrated passives seed layer	Ti (500-3000A) - Cu (2000-5000A)
Ti-Al	Aluminum RDL	Ti (100-300A) – Al (2-3 μm)
Ti-NiW-Cu Ti(W)-Ni	Ball drop UBM C4NP	Ti (1000-2000A) – NiW (2000-4000A)-Cu (4000-8000A) Ti(W) (1000-2000A) – Ni (1-2 μm)

TABLE 1. Typical UBM stacks used for various applications.

Secondly, the wafer is sputter cleaned using a mild argon plasma bombardment to remove oxides from the metal surface. The pre-clean etch, typically an inductively-coupled plasma (ICP) operating at low bias voltage (<150 volts) to avoid device damage, also improves ad-

hesion to the dielectric.

Barrier Function

TiW is generally deposited from targets with composition of 10% Ti and 90% W, and the deposited film is 5-7% Ti by weight so its material properties

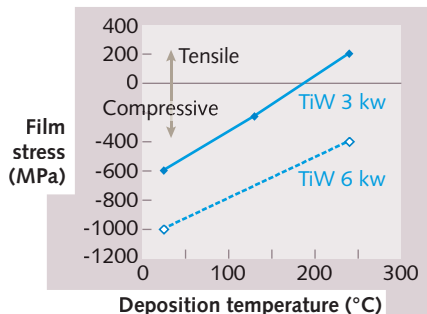


FIGURE 2. TiW film stress versus deposition temperature for 9 mTorr deposition pressure.

and sputtering behavior are dominated by the tungsten. Gold and copper atoms have low W diffusivity, so it provides reliable isolation between device pads and the bump or line that will be formed on top of the PVD layer. Ti is co-sputtered with W to provide better adhesion properties to the TiW film; therefore, this adhesion/barrier layer is found in applications such as gold-bump to aluminum pad where reliability would otherwise be degraded by gold migrating into the aluminum. Ti alone doesn't have comparable barrier properties, so it is found as the adhesion layer in applications, such as Cu-RDL to a Cu-pad, which will not be degraded by diffusion or in applications where another layer on top of the titanium, such as thick nickel (either PVD or electroplated) or thick copper (electroplated), will perform the barrier function.

A second aspect of barrier functionality is the requirement for a continuous film. In many cases, the PVD layer will be deposited into a feature with a high-aspect ratio or with an edge, such as where the dielectric material meets the bond pad surface. The deposition process must be controlled to ensure a continuous film that does not crack due to grown-in stresses.

UBM Frction

Under bump metal (UBM) is a general

Adhesion layer	Etchant	Etch of Other Important Metals					
		Cu	Ni	PbSn	SnAg	Al	Au
Ti	HF	N	N	Y	Y	Y	N
Ti	BOE	N	N	Y	Y	Y	N
Ti	H ₂ O ₂ -NH ₄ OH	N	N	Y	Y	Y	N
TiW	H ₂ O ₂	N	N	N	N	N	N

TABLE 2. Commonly used etchants for Ti and TiW.

term which may be applied to the whole metal stack under a solder or gold bump, including the Ti or TiW layers. More specifically, it refers to the metal, some of which will react to form intermetallic phases that bind the bump to the device pad while prohibiting further reaction or diffusion of the bump material into the device pad.

The entire UBM layer may be applied during the PVD operation, as is the case with a Ti/Ni UBM used for solder ball drop or C4NP processes. Or it may be applied as part of the solder application, for example, a stack of approximately 3-µm layers of copper and nickel electro-plated into the resist frame prior to electro-plating the solder itself.

In gold bumping, where TiW/Au, 3000A/1000A is typically used, the TiW acts as the adhesion, barrier, and UBM metal, although, unlike in solder UBMs, the gold doesn't form intermetallic phases with the TiW.

Etching of the Adhesion/Barrier Layer

Where the PVD layer is used as an electroplated seed layer, it remains continuous until after the patterned metal is applied and resist is stripped, at which point it is etched, using the applied thick metal as a mask. Where the PVD layer is patterned prior to thick metal application, it is photoresist patterned and then etched. Wet chemical etch is typically used because it avoids unwanted redeposition of the lower metal onto the side walls of upper layers of metal, or resist pattern, and it is a less expensive process, particularly for thick layers.

An important factor in determining which adhesion layer is used for the process is the compatibility of the etch process with metals exposed during etch; the adhesion layer etchant choice is restricted such that it minimally attacks the pri-

mary metals. The adhesion layer is masked by the PVD metal directly above it and must not react with etchants in a manner that will cause undercutting or accelerated lateral etching of the Ti or TiW at the

interface to adjacent metal. Ti has electrochemical activity of -1.63 volts, very close to Al at -1.66 volts, so it will etch similarly to Al, whereas W oxidizes less readily, having oxidation potential of -0.10 volts (compare to Sn -0.14, Pb -0.15, Ni -0.25, Cu +0.34, Au +1.50 Volts). Improvements in etch control and uniformity provided by etch tool design can also widen the process control window and allow more latitude in the choice of adhesion layer. Table 2 shows common etchants and their compatability with other metals of interest.

PVD Process Effects on Ti and TiW

Primary PVD control parameters are the magnetron and chamber design, deposition pressure, deposition power, film thickness, and wafer temperature. The properties of the top layer film, (Cu, Au, Ni), can also be used to optimize the overall stack properties.*

Film stress is a key parameter to control for barrier and adhesion properties. Highly stressed films will have poor adhesion and can flake, leading to high particle levels. Film stress is a combination of intrinsic and thermal stresses. As the film grows, intrinsic stress results from a proportion of atoms being in non-equilibrium lattice sites. Intrinsic compressive stress results from metal atoms being jammed into interstitial lattice sites; the film must expand for these atoms to move to lower energy lattice sites. Intrinsic tensile stress results from a high concentration of vacancies in the metal lattice. Therefore, to achieve equilibrium, the film must absorb vacancies and contract. The final film stress is the combination of the intrinsic stress and the thermal contraction mismatch to the silicon as the wafer cools from deposition to room temperature. Most metals are stretched by the wafer as they cool relative to silicon; Ti

shrinks about twice as much as TiW.

A significant difference between Ti and TiW PVD is that typically, Ti is tensile and TiW is compressive. For all metals, there is a transition operating pressure below which the film stress is compressive and above which it is tensile. The compressive to tensile transition occurs at a higher pressure for heavier metals like W than for light metals such as Ti, because it takes more argon working gas atoms to scatter and remove energy from the more massive impinging W atoms (Figure 1).

This compressive stress effect is referred to as atomic “peening”. Increasing the deposition rate, at a given pressure, increases the energetic particle bombardment and thereby increases the intrinsic stress. These effects occur for all metals when the deposition temperature, T_{dep} , is small compared to the melting point of the metal, T_{melt} . When $T_{\text{dep}}/T_{\text{melt}} < 0.25$, the mobility of the metal atoms is low and the films grow with a columnar structure. For a 150°C deposition temperature $T_{\text{dep}}/T_{\text{melt}} = 0.25$ for Ti and $T_{\text{dep}}/T_{\text{melt}} = 0.12$ for W, another reason TiW is in a more compressive regime.

Barrier properties degrade at higher pressure as the film begins to have voids and incorporate Ar into the film; therefore, the deposition pressure is usually kept below 10-11 mT. Thus, there is a trade-off between good barrier properties and acceptable stress. To operate at higher power deposition, the stress can be controlled by depositing at higher wafer temperature, both increasing $T_{\text{dep}}/T_{\text{melt}}$ and creating more tensile thermal stress

to offset some of the intrinsic compressive stress of the TiW film (Figure 2).

Applying an RF-bias adds ion and neutral particle bombardment of the surface, enhancing this effect by knock-on implantation of metal atoms into the film, producing a dense, compressive film. Because Ti is deposited on the tensile side of the pressure transition point, RF bias can be added to increase compressive intrinsic stress, and thereby make the final stress neutral.

The total stress of a TiW-Au or TiW-Cu stack can be controlled using the tensile stress of the seed metal (Au or Cu) to balance the compressive stress of the TiW. For example, the TiW in a TiW (2000Å) – Cu (3000Å) stack can be deposited at 5 mT with a stress of -650 MPa and combined with a Cu stress of +90 MPa, which produces a net stack stress of -30 MPa. For typical TiW-Au applications, this is less effective since the Au layer is typically much thinner than the TiW layer.

At typical operating power and pressure, Ti is on the tensile side of the stress

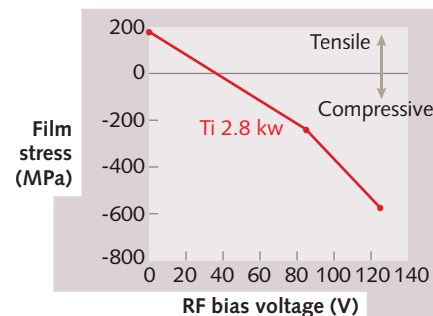


FIGURE 3. The dependence of Ti stress on RF bias power for a Ti deposition at 3 mT and 2.8 kW.

transition region. Ti stress can be reduced toward zero by increasing the intrinsic compressive stress by increasing the deposition power (rate), lowering the deposition pressure, or by “peening” the surface with RF bias. Ti is advantageous for processes requiring low wafer temperature, since it isn’t necessary to add more tensile thermal stress to offset an intrinsic compressive stress (Figure 3).

Conclusion

PVD-deposited Ti and TiW are commonly used as adhesion and barrier layers in many advanced packaging applications. The choice of which metal to use depends on both the materials properties and reactions with adjacent metals, as well as compatibility with subsequent processing operations. PVD deposition systems designed for advanced packaging applications provide the economical COO needed to keep these exciting new technologies growing. **AP**

*A summary comparison of parameters for Ti and TiW films is available in the online version of this article.

REFERENCES

Contact the authors for a complete list of references.

ARTHUR KEIGLER, V.P. technology; STEPHEN GOLOVATO, Ph.D. manager, process engineering, Nimbus/Cirrus; KATHY O’DONNELL, Ph.D. director of business development; JOHANNES CHIU, Ph.D., senior electrical engineer, and RICHARD HOLLMAN, Ph.D., senior process engineer may be contacted at NEXX Systems, 5 Suburban Park Drive, Billerica, MA 01821; 978/932-2001; E-mail: arthur_keigler@nexxsystems.com.