

## Advances in Metal Deposition for Wafer Bumping

### Increasing Complexity and Functionality of Packages

BY MATT DOROGI, MARK WELSH, AND ARTHUR KEIGLER

The semiconductor manufacturing process involves two distinct phases: wafer processing — or “front-end” — and assembly operations — or “back-end” — which includes wire bonding, bumping, packaging, and test. It is critical for manufacturers to protect their front-end investment in finished wafers during the packaging process by increasing throughput, minimizing scrap, and shortening manufacturing lead times.

Technological developments in the front-end have created a need for new packaging solutions, placing increased pressure on back-end equipment manufacturers. Processing and handling of ultra-thin wafers in back-end packaging tools are a result of device form factor requirements for die-stacking and chip scale packages. Environmental concerns, such as lead-free legislation, also drive tool process advances in the back-end.

Wafer bumping is a key component of advanced packaging, both from a cost and technology point of view. Metal deposition accounts for 50% or more of the total cost in wafer bumping. The most common metal deposition steps in wafer bumping are under-bump metallization (UBM) and deposition of the bump itself, often by electroplating.

#### Metal Deposition for Wafer-level Packaging

Many of the process requirements for metal deposition in wafer-level packaging are similar to those in the front-end. Process throughputs must be in the 35- to 45-wph range. Within-wafer and wafer-to-wafer non-uniformity specifications are <5% for wafer bumping. Particle requirements are relaxed because of the larger feature sizes, with most manufacturers only concerned about particles greater than 1 µm.

Back-end metal deposition tools are not required to address the process requirements of the front-end, such as filling high aspect contacts and vias with sub-micron fea-

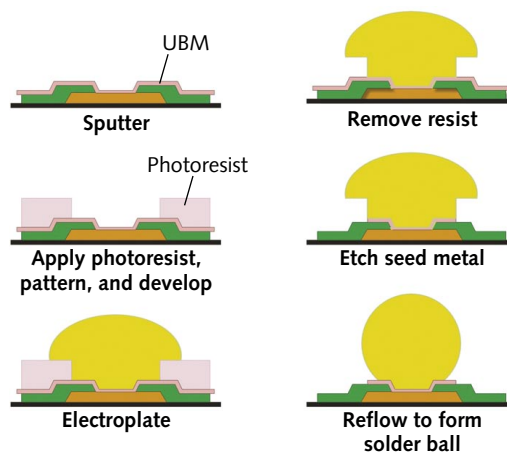


Figure 1. Process flow for wafer bumping.

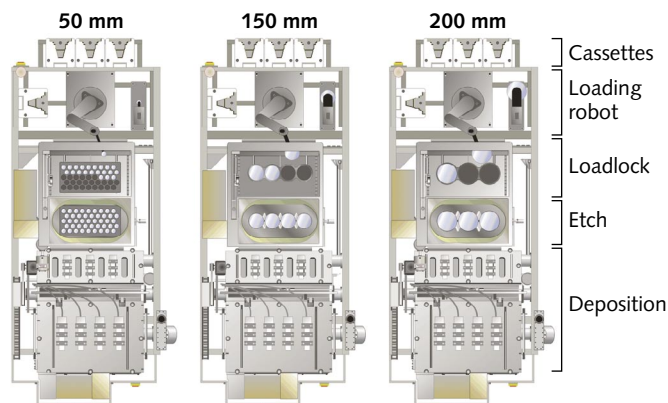
tures. Rather, they are required to be much more versatile. While front-end metal deposition tools are usually designed for a particular wafer size and technology node, back-end metal deposition tools must be capable of handling all wafer sizes. Packaging operations may not be profitable if they have to buy multiple tool sets for different wafer sizes. Most packaging foundries run wafer sizes ranging from 150 to 300 mm. Considering the packaging requirements for compound semiconductors such as LEDs, the size range can vary from 50 to 300 mm. Back-end metal deposition tools are required to have the same process performance, the same throughput, and more wafer-size versatility.

While the 300-mm transition led to the design of 200- to 300-mm bridge tools, foundries haven’t seen any front-end tools with such versatility in handling different wafer sizes. This requirement has led to the development of low-cost, high-performance metal deposition tools capable of handling multiple wafer sizes in full-volume production, with 2-hour conversion time.

Figure 1 shows a typical process flow for wafer bumping. Incoming wafers are first coated with UBM layer. A thick photoresist layer is deposited and exposed, forming a template for solder plating. After plating, the resist is stripped and the exposed UBM is etched away. The final step is a reflow process that forms the solder ball.

#### Under-bump Metallization

The UBM layer is the critical interface between the IC metal pad and the gold or solder bump used for the flip chip connection. This layer is one of the key components of flip



**Figure 2.** Architecture of a metal deposition tool designed for wafer-level packaging. The same tool is capable of handling wafers from 50 to 300 mm, with a size conversion time of 2 hours or less.

chip packaging and is necessary to create a highly reliable electrical and mechanical interface between the chip's circuitry and the solder bumps. The UBM layer between the bump and the I/O pad should provide excellent adhesion to the metal pad and wafer passivation layer; protect the metal pad from subsequent processing steps; have low contact resistance between the metal pad and the bump; be an effective diffusion barrier between the metal pad and bump; and act as a good seed layer for solder- or gold-bump deposition.

The UBM layer is typically a multi-layer stack of metals deposited over the entire wafer surface. Several techniques used to deposit the UBM layer include evaporation, electroless plating, and sputter deposition.

The C4 process is good example of evaporation technology that has been used in manufacturing for years. Most evaporators are manually loaded and not well-suited for high-volume applications. Evaporation is not easily scaled to larger wafer sizes — a critical requirement for wafer-level packaging. The low throughput and high cost of evaporation tools limits their use. Evaporation is still used for backside metal applications, but as wafers are thinned below 100  $\mu\text{m}$ , manual handling of wafers and wafer breakage have become serious issues.

Electroless plating is a promising technology for UBM. It can reduce costs through elimination of masking and metal deposition steps required by other methods, and can be scaled to multiple wafer sizes. However, electroless

plating does have drawbacks. Any exposed metal, aside from the pads, must be passivated or protected with photoresist. The back side of the wafer may also need protection. Reliability concerns with electroless plating include poor adhesion to the passivation

layer and high film stress in the UBM layer. It can also be unstable, which is an issue for high-value products. Losing an entire lot of high-value wafers is a risk some manufacturers will not take. Elec-

trons for wafer-level packaging have become more prevalent and include both cluster and batch tools. Cluster tools offer the necessary process performance but are higher in cost. Converting from one wafer size to another is generally more difficult with a cluster tool. Batch tools cost less than cluster tools and are easier to maintain, but their throughput is lower. They are best-suited for specialized, low-volume applications. Hybrid tools, which combine cluster-tool throughput and performance with the low cost of batch tools, are becoming more popular. Figure 2 shows the architecture of a tool designed specifically for back-end metal deposition. Wafers are loaded onto trays and processed in batches, which allows for more versatility in handling multiple wafer sizes, thinned wafers, and wafers on carriers.

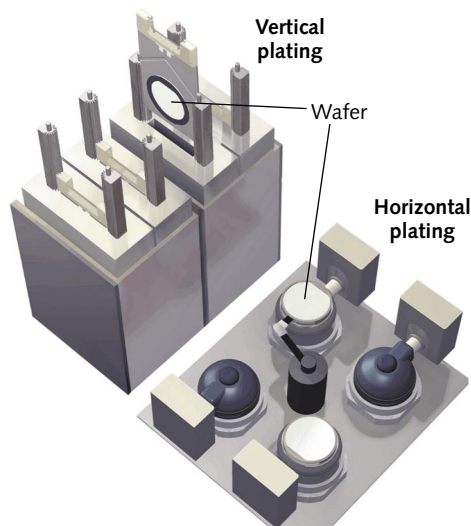
### Wafer-bump Deposition

Evaporation, stencil printing, and plating are the three most common technologies used for depositing the wafer bump. Evaporation suffers from the same drawbacks for bump deposition as it does for UBM. High costs and low throughput limit the use of evaporation for bump deposition in high-volume manufacturing.

In stencil printing, solder paste is printed on to the UBM by screening it through a stencil. The stencil contains apertures that align with the wafer bond pads. The solder paste is transferred to the bond pads by pushing a bead of solder across the stencil. The stencils can be made using a variety of methods, including laser cutting, masking, and photolithography.

Stencil printing is a straightforward and inexpensive technology that can be used with almost any solder alloy, which is an advantage for lead-free solder requirements. For fine-pitch applications (below 200  $\mu\text{m}$ ), yield loss becomes an issue for stencil printing, and eliminates its cost-effectiveness. Stencil printing may reach practical limits with increasing bump density and device performance requirements.

Considering tool and materials cost, stencil printing is the lowest-cost method of depositing bumps. However, if



**Figure 3.** Comparison of vertical (left) and horizontal (right) electroplating cells. Two wafers can be processed in a single vertical cell, which gives it a 2 to 4x capacity advantage over a horizontal cell.

troless plating for UBM is typically used for low-end products where yield is not an issue.

Sputtering offers the best combination of film uniformity, throughput, and cost for UBM deposition. Sputtering is cost-effective, scaleable, and production-worthy. Some large IDMs re-use front-end sputter equipment for UBM deposition, but the cost of this equipment is too high for most manufacturers.

Over the last few years, physical vapor deposition (PVD) tools designed specifi-

Electroplating is the most versatile process, relative to bump size, pitch, and geometry, and is increasingly used **in wafer bumping**.

yield loss is factored, electroplating becomes a much more practical solution. Electroplating can accommodate tight bump pitches and maintain high yield. It is the most versatile process, relative to bump size, pitch, and geometry, and is increasingly used in wafer bumping.

As in the case for UBM deposition, requirements for front- and back-end plating tools are different. Front-end plating tools were developed for copper damascene structures, while bumping requires multi-metal pattern structures with thickness values up to 100  $\mu\text{m}$ . These bumps require long deposition times and have driven the development of tools to meet the cost and throughput requirements of back-end packaging.

Two basic architectures have been employed in bump plating: hori-

zontal “fountain-cell” and vertical “rack” plating tools. Horizontal bump-plating tools evolved from front-end copper damascene processes and incorporate much of the process control and ancillary equipment, such as chemical delivery, resulting in a high level of tool complexity and cost-of-ownership.

Vertical plating tools have a capacity advantage over horizontal plating tools, particularly for 300-mm wafers. The wafer throughput of a vertical plating tool can far exceed that of a horizontal fountain cell tool because multiple cells fit into the space that a single horizontal fountain cell would occupy (Figure 3). A vertical electroplating cell can process two wafers at a time, giving a capacity that can be 2 to 4 $\times$  that of a horizontal electroplating cell with a similar footprint. In addition,

vertical electroplating tools with the capability to simultaneously process different-size wafers have been developed.

### Conclusion

Methods used for metal deposition in advanced packaging are similar to those used in the front-end, with PVD and electroplating making up the majority of the market. Economic and technology requirements are driving the development of new equipment designed specifically for wafer-level packaging. These tools must handle multiple wafer sizes in production, while maintaining the same throughput and lower cost than comparable front-end metal deposition tools. **AP**

---

MATT DOROGI, Ph.D., product manager, Nimbus; MARK WELSH, product manager, Stratus; and ARTHUR KEIGLER, VP of technology, may be contacted at NEXX Systems Inc., 5 Suburban Park Dr., Billerica, MA 01821-3904; 978/932-2029; E-mail: Matt\_Dorogi@nexxsystems.com.



NEXX Systems brings exceptional technical expertise to flip chip and advanced packaging, including gold bumping, aluminum redistribution, and LEDs. Our product lines provide the most efficient, yet affordable, systems of their kind:

- Nimbus for multi-layer sputter deposition of metals



- Stratus for high throughput electro-deposition of metals



Additional information can be found at: [www.nexxsystems.com](http://www.nexxsystems.com).